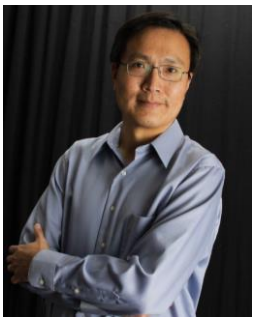
课程名称:　VLSI/FPGA 物理设计自动化基础

英文名称: Fundamentals of VLSI/FPGA Physical Design Automation

课程编号: X2EI1001



开课单位：卓越工程师学院

开课企业: 上海思尔芯技术股份有限公司

主讲人: 孙亚强 （Richard Y. Sun, Ph.D）

(CTO, 首席技术官）

学时: 32

学分: 2

上课时间：10 月 10 日开始，每周二、四晚。

上课方式：线上线下结合。部分课时线下授课，部分课时线上授课。

选课方式： 在“我的培养计划”中点击“课程库选课”搜索名称或者课程编号，再在“我的选课”中选定班级。

备注：目前暂未确定具体的上课教室，待正式开始上课前会更新到课表中。

咨询电话： 81891044

课程概况-Course Description

Physical design is the phase that follows logic design, and it includes the following steps that precede the fabrication of the IC: logic partitioning, cell layout, floorplanning, placement, and routing. In this course, the automation of these steps is examined in the context of very deep submicron technology. We shall also discuss the applications of several important optimization techniques, such as network flow, Steiner tree, scheduling, simulated annealing, genetic algorithm, and linear/convex programming.

课程教学目标-Course Objective

- Understand the concepts of physical design process such as partitioning, floorplanning, placement, routing, and timing optimization.
- Discuss the concepts of basic design optimization algorithms and their applications to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI/FPGA Design Automation.
- Formulate CAD design problems using algorithmic methods.

课程要求：

建议在本科阶段学过“计算机算法设计与分析”的课程或同等课程，能够基本掌握基本算法知识、逻辑电路、集成电路、C++、Java 或 Python 编程技能的知识。

教辅材料-Required Reading Materials –

[1]. **(Required Textbook)** Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu. VLSI Physical Design: From Graph Partitioning to Timing Closure. Springer; 2011th edition, February 9, 2011. ISBN: 978-9048195909.

[2]. Class notes and published papers.

教学内容与课时安排

课次 （每次 2 学时）	主题	教辅材料
1	**Basic Concepts**	[1] Ch.1
2-4	**Netlist Partitioning**	[1] Ch. 2
5-6	**Chip Planning**	[1] Ch. 3
7-8	**Placement**	[1] Ch. 4
9-10	**Global Routing**	[1] Ch. 5
11	**Detailed Routing**	[1] Ch. 6
12	**Specialized Routing**	[1] Ch. 7

13	**FPGA Routing**	[2]
14-15	**Timing Closure**	[1] Ch. 8
16	**Demo of Students' Programming Assignments**	

预期学习成效：Expected Learning Outcomes –

By the end of the course, students should be able to:

CO1: know how to place the blocks and how to partition the blocks for designing the IC layout.

CO2: solve the basic performance issues in circuit layout.

CO3: analyze basic physical design problems and employ appropriate automation algorithms for partitioning, floor planning, placement, and routing.

CO4: decompose a large mapping problem into pieces, including logic optimization with partitioning, placement, and routing.

CO5: analyze circuits using both analytical and CAD tools。